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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,549	04/08/2004	Ramesh Peri	ITL.01491US (P18223)	1329

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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,549	PERI ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 4 recites the limitation "... to detect whether the address value has been incremented or decremented". This limitation is unsupported by the specification, which only teaches detecting whether the system is in pre/post incremented/decremented address mode or not, not detecting whether the address value has been incremented or decremented (see specification, page 8, paragraphs [0027]-[0028] and page 11, paragraphs [0030]+[0032). Detection of addressing mode is not equivalent to the detection of the type of change to the address value. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 and 7-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Mayfield et al. [US 6,535,962 B1] (hereinafter "Mayfield").

Per claims 1 and 7-9, Mayfield teaches a processor (the processing unit containing microprocessor, L2 and L3 caches; see col. 4, lines 3-23) comprising:

a cache memory to store a plurality of data (L2 and/or L3 cache, see Fig. 1 and 2);

a processor core to generate addresses corresponding to data stored within the cache memory (addresses that match cache lines in L2) ;

a plurality of buffers (cache lines in L1) from which the processor core may retrieve copies of data stored within the cache memory, the plurality of buffers being associated with a plurality of locations within the cache memory (the prefetched caches lines from L2 into L1 that match the processor addresses are used to service the processor requests instead of the cache lines in the L2 cache; see col. 2, lines 51-64 and col. 5, lines 1-14).

It is clear the apparatus of claims 1, 7 and 8 are disclosed by the processor taught by claim 9.

Per claim 10, Mayfield further teaches a selection unit to select one of the plurality of buffers from which to retrieve data (there must be a unit to select the L1 cache lines that are hit by the addresses).

Per claim 11, Mayfield further teaches aligning and signing logic to appropriately shift and apply appropriate sign information to data stored within the buffer selected by the selection unit (processors have shifters and sign-extension functional units).

Per claim 2, 3 and 12, Mayfield further teaches a buffer control unit to detect whether an address generated by the processor core corresponds to data stored within any of the plurality of buffers, and if so, to select data within the plurality of buffers to which the address generated by the processor core corresponds (processor requests result in checking the L1 cache first for a hit, if the requested data has been prefetched or otherwise already exists in L1, the request is serviced by the L1 cache; see col. 2, lines 51-64 and col. 5, lines 1-14).

Per claim 13, Mayfield further teaches validation indicators to indicate whether data stored within the load buffers is valid (L1 cache entries have valid bits for indicate that the entries are valid for tag comparison).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 and 5 are rejected under 35 U.S.C 103(a) as being unpatentable over Mayfield, in further view of Dent [US 6,314,504 B1] (hereinafter "Dent").

Per claims 4 and 5, Mayfield does not teach that the buffer logic comprises overflow detection logic to detect whether the address value has been incremented or decremented and an arithmetic unit to increment or decrement the address value. However, Dent teaches a post-increment mode and a pre-decrement addressing mode in a microprocessor. The addressing modes give "advantages when ... an array of data in memory is to be accessed sequentially" by automatically increment or decrement the address values after or before use of the address values (see col. 4, lines 33-46). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the applicant's invention to include post-increment and pre-decrement addressing modes in Mayfield's processors to provide advantage when accessing arrays of memory data sequentially. As a result, Mayfield in combination with Dent teaches that the buffer logic comprises overflow detection logic to detect whether the address value has been incremented or decremented and an arithmetic unit to increment or decrement

the address value. The mode selection bits taught by Dent detect whether the address value has been incremented or decrement.

7. Claims 6 and 14-17 are rejected under 35 U.S.C 103(a) as being unpatentable over Mayfield, in further view of Patterson and Hennessy [Computer Architecture A Quantitative Approach] (hereinafter "Patterson").

Per claims 6, 14 and 15, Mayfield does not teach the validation indicators are to indicate that data within all of load buffer is invalid if the processor core has performed or will perform a write operation to a location within the cache memory to which a load buffer corresponds. However, Mayfield teaches a multiprocessor system with shared L2 and L3 caches and distributed L1 caches (see Mayfield, Fig. 1). Patterson teaches write invalidate protocol in a multiprocessor system with distributed cache to maintain coherency (see Patterson, pages 658-666). The write invalidate protocol invalidates other copies of cache lines when a processor writes to its own copy of the cache lines to gain exclusive access and achieve cache coherency (here the other copies of cache are considered to be all of the load buffers). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the applicant's invention to use the write invalidate protocol to maintain cache coherency in Mayfield's system by invalidating other copies of cache lines when a processor writes to its own copy of the cache lines.

Per claims 16 and 17, Mayfield teaches a plurality of tag storage units to store portions of the cache memory address to which the load buffers correspond (see Mayfield, Fig. 1, a cache line must have a tag portion for determination of cache hit/miss), and further teaches a comparator unit to compare contents of the tag storage unit to a portion of a cache memory address generated by the processor core (processor generated address is compared to the tag portion of the cache line to determine hit/miss).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

26 February 2007